WHAT IS CLAIMED IS:

1. An active matrix backplane used within a display, comprising:

a plurality of pixels; and

a plurality of pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels, wherein each pixel transistor within said plurality of pixel transistors is a nanowire transistor.

2. The active matrix backplane of claim 1, wherein each nanowire transistor comprises at least two nanowires extending at least between a source and a drain electrode.

3. The active matrix backplane of claim 1, wherein each nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a respective pixel at a desired rate.

4. The active matrix backplane of claim 1, further comprising a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of said plurality of pixel transistors, wherein each column transistor within said plurality of pixel transistors is a nanowire transistor.

5. The active matrix backplane of claim 4, wherein each column nanowire transistor comprises at least two nanowires extending at least between a source and a drain electrode.

6. The active matrix backplane of claim 4, wherein each column nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a respective pixel at a desired rate.

7. The active matrix backplane of claim 1, further comprising a plurality of row transistors, wherein a row transistor within said plurality of row transistors applies a voltage across a subset of said plurality of pixel transistors, wherein each row transistor within said plurality of row transistors is a nanowire transistor.

8. The active matrix backplane of claim 7, wherein each row nanowire transistor comprises at least two nanowires extending at least between a source and a drain electrode.

9. The active matrix backplane of claim 7, wherein each row nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a respective pixel at a desired rate.

10. The active matrix backplane of claim 1, further comprising nanowire edge electronics.

11. The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire buffers.

12. The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire shift registers.

13. The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire level shifters.

14. The active matrix backplane of claim 1, wherein the display is a liquid crystal display.

15. The active matrix backplane of claim 1, wherein the display is an organic light emitting display (OLED).

16. The active matrix backplane of claim 15, wherein said OLED includes nanocrystals.

17. The active matrix backplane of claim 1, wherein the display is an electrophoretic display.

18. The active matrix backplane of claim 1, wherein the display is a plasma display.

19. The active matrix backplane of claim 1, wherein the display is an electrochromic display.

20. The active matrix backplane of claim 1, wherein the display is a microelectromechanical (MEMs) display.

21. The active matrix backplane of claim 1, wherein the display is a micromirror display

22. The active matrix backplane of claim 1, wherein the display is a field emission display.

23. The active matrix backplane of claim 22, wherein the display is a nanotube field emission display.

24. The active matrix backplane of claim 1, wherein the display is rigid.

25. The active matrix backplane of claim 1, wherein the display is flexible.

26. The active matrix backplane of claim 1, wherein the display is non-planar.

27. A liquid crystal display having a base substrate comprising:
    (a) a plurality of pixels;
    (b) a plurality of pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels;
    (c) a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of said plurality of pixel transistors; and
    (d) a plurality of row transistors, wherein at least two row transistors within said plurality of row transistors turns a corresponding pixel transistor on and off, wherein at least one of said plurality of pixel transistors, said plurality of column transistors, and said plurality of row transistors are nanowire transistors.

28. The liquid crystal display of claim 27, further comprising nanowire edge electronics.

29. The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire buffers.

30. The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire shift registers.

31. The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire level shifters.

32. The liquid crystal display of claim 27, wherein pixel transistors within said plurality of pixel transistors, column transistors within said plurality of column transistors, and row transistors within said plurality of row transistors are nanowire transistors.

33. The liquid crystal display of claim 27, wherein at least one of said plurality of pixel transistors, said plurality of column transistors, and said plurality of row transistors are a-Si thin film transistors.

34. The liquid crystal display of claim 27, wherein at least one of said plurality of pixel transistors, said plurality of column transistors, and said plurality of row transistors are bulk Si thin film transistors.

35. The liquid crystal display of claim 27, wherein at least one of said plurality of pixel transistors, said plurality of column transistors, and said plurality of row transistors are organic semiconductors.

36. The liquid crystal display of claim 27, wherein at least one of said plurality of pixel transistors, said plurality of column transistors, and said plurality of row transistors are poly-Si thin film transistors.

37. The liquid crystal display of claim 27, wherein nanowires used to form the transistors are aligned substantially parallel.

38. The liquid crystal display of claim 27, wherein the wires are aligned one of substantially randomly and isotropically.

39. The liquid crystal display of claim 27, wherein nanowire column transistors are located between column traces.

40. The liquid crystal display of claim 27, wherein nanowire column transistors are located inline with the column traces.

41. The liquid crystal display of claim 27, wherein nanowire row transistors are located between row traces.

42. The liquid crystal display of claim 27, wherein nanowire row transistors are located inline with row traces.

43. The liquid crystal display of claim 27, wherein each nanowire transistor comprises at least two nanowires.

44. The liquid crystal display of claim 27, wherein a nanowire transistor comprises at least ten nanowires connecting a source to a drain electrode of the nanowire transistor.

45. The liquid crystal display of claim 27, wherein a nanowire transistor comprises at least one hundred nanowire connecting a source to a drain electrode of the nanowire transistor.

46. The liquid crystal display of claim 27, wherein the base substrate is a flexible material.

47. The liquid crystal display of claim 27, wherein the base substrate is a low temperature material with a melting temperature below 500 degrees Fahrenheit.

48. The liquid crystal display of claim 27, wherein the base substrate is a plastic.

49. The liquid crystal display of claim 27, wherein the base substrate is translucent material.

50. An nanowire pixel transistor, comprising:

(a) at least one nanowire,

(b) a row electrode that connects said at least one nanowire to a row trace;

(c) a gate electrode that connects said at least one nanowire to a column line trace; and

(d) a pixel electrode that connects said at least one nanowire to conductive material used to apply a voltage across a pixel.

51. The nanowire pixel transistor of claim 50, wherein the pixel electrode connects at least two nanowires to the conductive material.

52. An active matrix backplane used within a display, comprising:

a plurality of pixels;

a plurality of amorphous silicon pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels; and

a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of said plurality of pixel transistors, and wherein each column transistor within said plurality of pixel transistors is a nanowire transistor.

53. The active matrix backplane of claim 52, wherein each nanowire transistor comprises at least two nanowires extending at least between a source and a drain electrode.